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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant(s):	Cyril Cabral, Jr., et al.	**Examiner:**	Erik J. Kielin
Serial No:	09/994,954	**Art Unit:**	2813
Filed:	November 27, 2001	**Docket:**	YOR919990509US2(13171A)
For:	METHOD AND STRUCTURE FOR REDUCTION OF CONTACT RESISTANCE OF METAL SILICIDES USING A METAL-GERMANIUM ALLOY	**Dated:**	November 10, 2003

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DECLARATION OF CHRISTIAN LAVOIE UNDER 37 C.F.R. §1.132

Sir:

I, Christian Lavoie, hereby declare and say that:

(1) I am one of the applicants named in U.S. Application Serial No. 09/994,954, filed with the United States Patent and Trademark Office on November 27, 2001.

(2) The present invention is directed to a structure having metal silicides produced from a metal germanium alloy having a reduced contact resistance.

(3) I am familiar with the subject matter disclosed in U.S. Application Serial No. 09/994,954, filed November 27, 2001; and have reviewed the applied references, namely U.S. Patent No. 5,710,450 to Chau, et al. ("Chau, et al."), U.S. Patent No. 5,830,775 to Maa, et al. ("Maa, et al.") and of U.S. Patent No. 5,510,295 to Cabral Jr., et al. ("Cabral Jr., et al.") that were cited in the final Office Action dated September 10, 2003.

(4) I am familiar with the Examiner's comments in the final Office Action dated September 10, 2003. It is the Examiner's position that a SiGe interlayer can not be formed at the interface between the metal silicide and substrate. Specifically, the Examiner argues that the statement on Page 12, second paragraph, of the application disclosing that an "annealing

temperature range [of about 400°C to about 700°C] provides enough thermal energy to produce the SiGe interlayer by diffusing Ge to the interface between the metal silicide and the substrate; but does not provide enough energy to diffuse the Ge into the Si substrate" is an error. It is the Examiner's position that a Si-Ge interlayer cannot be produced up to 3.0 nm if Ge does not penetrate into the substrate. The Examiner continues that if diffusion does not occur into the substrate then the application is providing erroneous information regarding (1) the formation of Si-Ge; and (2) thickness of the Si-Ge interlayer. The Examiner further argues that since diffusion continues in three dimensions, the Ge would diffuse past the edges of the metal disilicide. In summary, it is the Examiner's position that the applicants have failed to disclose that the SiGe interlayer does not extend beyond the overlying metal disilicide since the application fails to disclose controlling the diffusion of Ge into the substrate.

(5) The Examiner's misconceptions regarding the diffusion of Ge and the formation of the SiGe interlayer can be clarified in the Example discussed on Pages 15-17 and FIGS. 4-5 of U.S. Application Serial No. 09/994,954. FIG. 4 is a TEM of a Co disilicide film made from a Co alloy having 2.1 atomic % Ge, where points A and B represent the points on which local analysis was performed. Point A is the Ge rich interlayer and Point B is in the disilicide layer. FIG. 5 is the EDX analysis (Normalized EDX Intensity, arb. units v. Energy, KeV) at Point A and Point B of FIG. 4. Exhibit A includes a duplicate copy of the original FIG. 4. Exhibit B includes a duplicate copy of original FIG. 5. Referring to Page 15, the Co disilicide disclosed in the examples section of the above referenced application was formed by depositing a Co-Ge alloy, having about 2 atomic % Ge, followed by a first anneal at a temperature of about 550°C followed by a second disilicide anneal at a temperature of about

800°C. Under these annealing conditions enough thermal energy is provided to produce the SiGe interlayer by diffusing Ge to the interface between the metal silicide and the substrate; but does not provide enough energy to substantially diffuse the Ge into the Si substrate. Although some Ge [in low concentration] may diffuse into the substrate, it is clear from the attached photograph in Exhibit A, which is a duplicate copy of the originally submitted FIG. 4, that the Ge diffuses from the deposited metal alloy forming the SiGe interlayer only at the interface between the metal disilicide and the substrate. It is further noted that silicon from the substrate intermixes with Ge forming the SiGe interlayer. Additionally, the Si further diffuses to form the metal silicide.

Exhibit A clearly depicts a SiGe interlayer from which a local analysis (EDX) measurement was taken at point A, where point A is substantially at the center of the SiGe interlayer. Exhibit A also clearly depicts that a metal disilicide is formed overlying the SiGe interlayer from which a local EDX measurement was take at point B. The results of the EDX analysis are depicted in Exhibit B where two Ge peaks where measured in the SiGe interlayer at point A. Exhibit B further indicates Ge peaks were not measured at point B representing the metal disilicide that the Ge was originally deposited in. Therefore, it is clear from Exhibits A and the EDX analysis at points B and A that the Ge diffuses to the interface between the metal disilicide and the substrate intermixing with interfacial Si to form the SiGe interlayer. Referring to Exhibit A, by using the 30.0 nm scale supplied it is clear that the SiGe interlayer has a thickness of less than about 3.0 nm. The region underlying and having a different contrast than the SiGe interlayer is the substrate. Although a slight amount of Ge may possibly diffuse into the substrate, if the Ge had uniformly diffused beyond the interface between the metal silicide and the substrate the SiGe interlayer would not be produced. In

summary, it has been clearly demonstrated that Ge originally deposited in the metal alloy layer diffuses to the interface between the metal disilicide and substrate in a concentration sufficient enough to form a SiGe layer having a thickness on the order of about 3.0 nm or less.

(6) All statements made herein, of my own knowledge, are true, and that all statements made on information and belief are believed to be true; and further that these statements are made with the knowledge that willful false statements and the like so made may be punishable by fine or imprisonment or both, under Section 1001 Title 18 of the U.S. code and that such willful false statements may jeopardize the validity of the application or any patent issuing therefrom.

Dated: November 10, 2003

Christian Lavoie